

REVISION HISTORY

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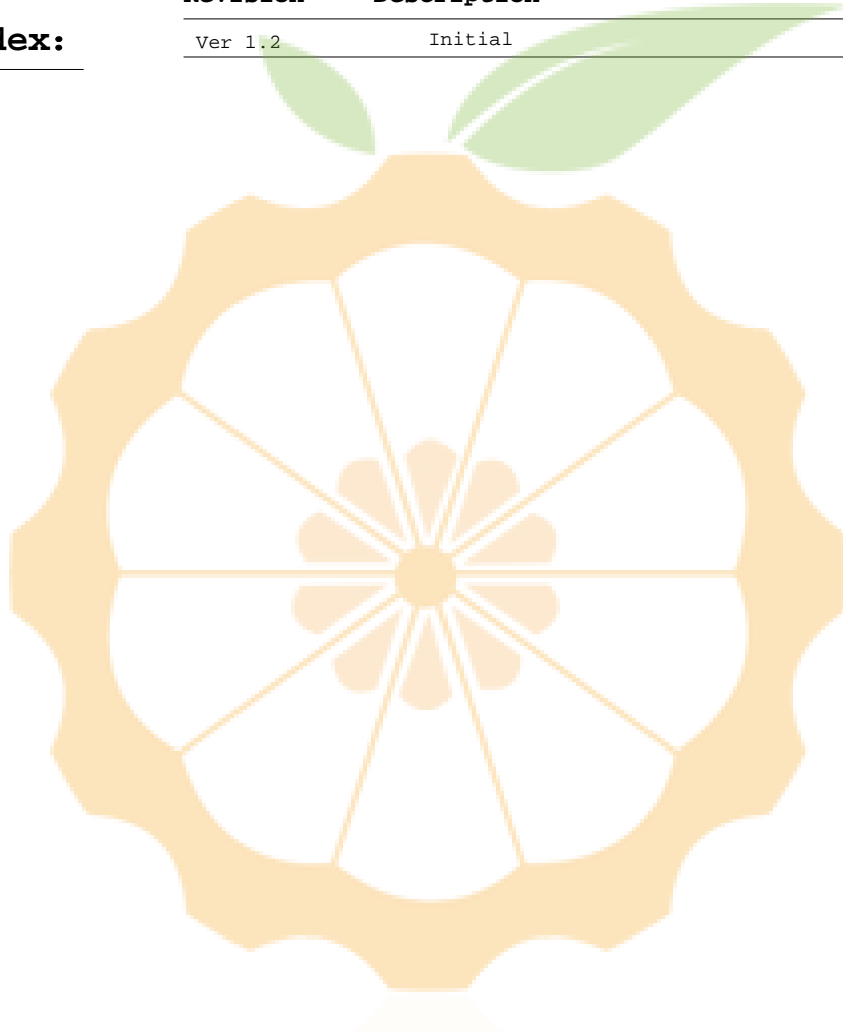
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2

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Schematics Index:

Revision	Description	Date	Drawn	Checked
Ver 1.2	Initial	2015-07-10		



D

D

C

C

B

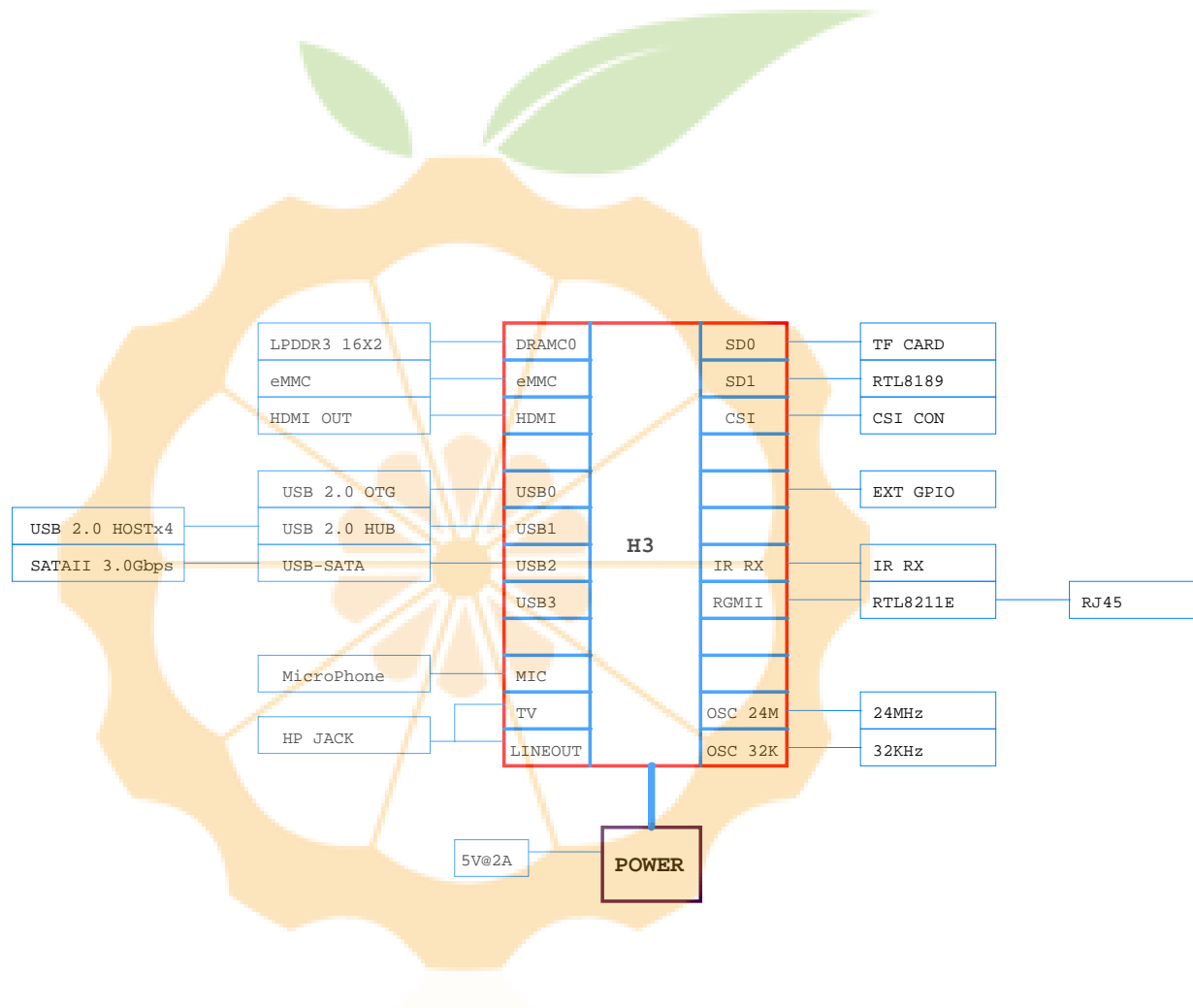
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A

A

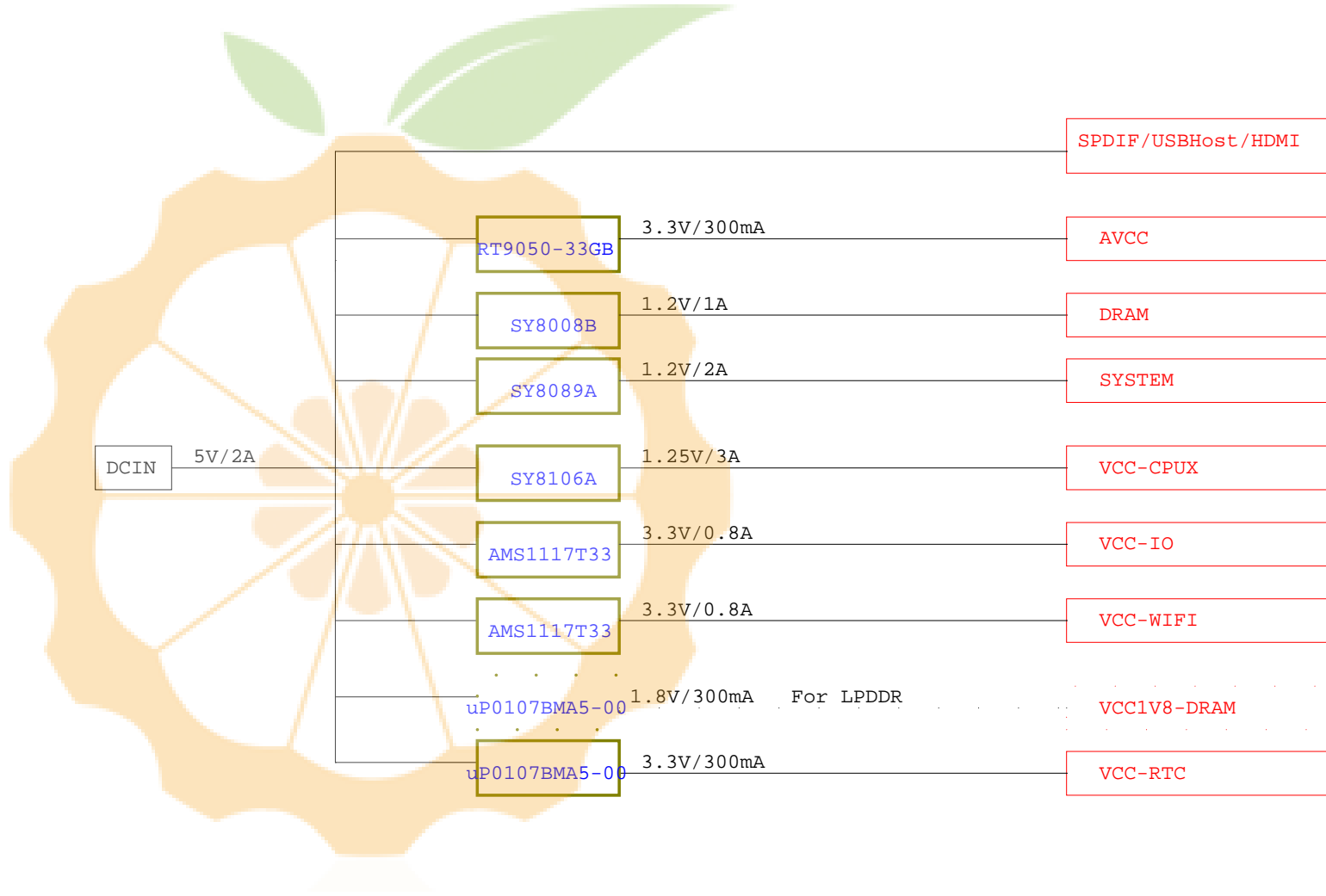
Xunlong Software		
Design Name		
ORANGE_PL_PC		
Size	Page Name	Rev
A3	REVISION HISTORY	
Date: Tuesday, September 08, 2015 Sheet 1 of 16		

BLOCK



Xunlong Software		
Design Name		
ORANGE_PI_PC		
Size	Page Name	Rev
A3	BLOCK	
Date:	Saturday, July 11, 2015	Sheet 2 of 16

POWER TREE



Xunlong Software		
Design Name		
ORANGE_PI_PC		
Size	Page Name	Rev
A3	POWER TREE	
Date:	Saturday, July 11, 2015	Sheet 3 of 16

GPIO ASSIGNMENT

PIN	Define	CFG	Function
PA0	DMS/DRVVBUS0	3/1	
PA1	CK/DRVVBUS1	3/1	JTAG /USB
PA2	TDO/WPS	3/1	
PA3	FDI	3	
PA4	JART-TX	3	UART
PA5	JART-RX	3	
PA6	NC	7	
PA7	NC	7	
PA8	NC	7	
PA9	NC	7	
PA10	NC	7	
PA11	NC	7	
PA12	NC	7	
PA13	NC	7	
PA14	NC	7	
PA15	STATUS-LED	1	LED
PA16	MUTE	1	AV
PA17	SPDIF-OUT	2	SPDIF
PA18	NC	7	
PA19	NC	7	
PA20	NC	7	
PA21	NC	7	

PIN	Define	CFG	Function
PC0	NWE	2/3	
PC1	NALE	2/3	
PC2	NCLE	2/3	
PC3	NCE1	2/3	
PC4	NCE0	2	NAND /eMMC /NOR
PC5	NRE	2/3	
PC6	NRB0	2/3	
PC7	NRB1	2	
PC8	NDQ0	2/3	
PC9	NDQ1	2/3	
PC10	NDQ2	2/3	
PC11	NDQ3	2/3	
PC12	NDQ4	2/3	
PC13	NDQ5	2/3	
PC14	NDQ6	2/3	
PC15	NDQ7	2/3	
PC16	NDQS	2/3	

PIN	Define	CFG	Function
PD0	NC	7	
PD1	NC	7	
PD2	NC	7	
PD3	NC	7	
PD4	NC	7	
PD5	NC	7	
PD6	NC	7	
PD7	NC	7	
PD8	NC	7	
PD9	NC	7	
PD10	NC	7	
PD11	NC	7	
PD12	NC	7	
PD13	NC	7	
PD14	NC	7	
PD15	NC	7	
PD16	NC	7	
PD17	NC	7	

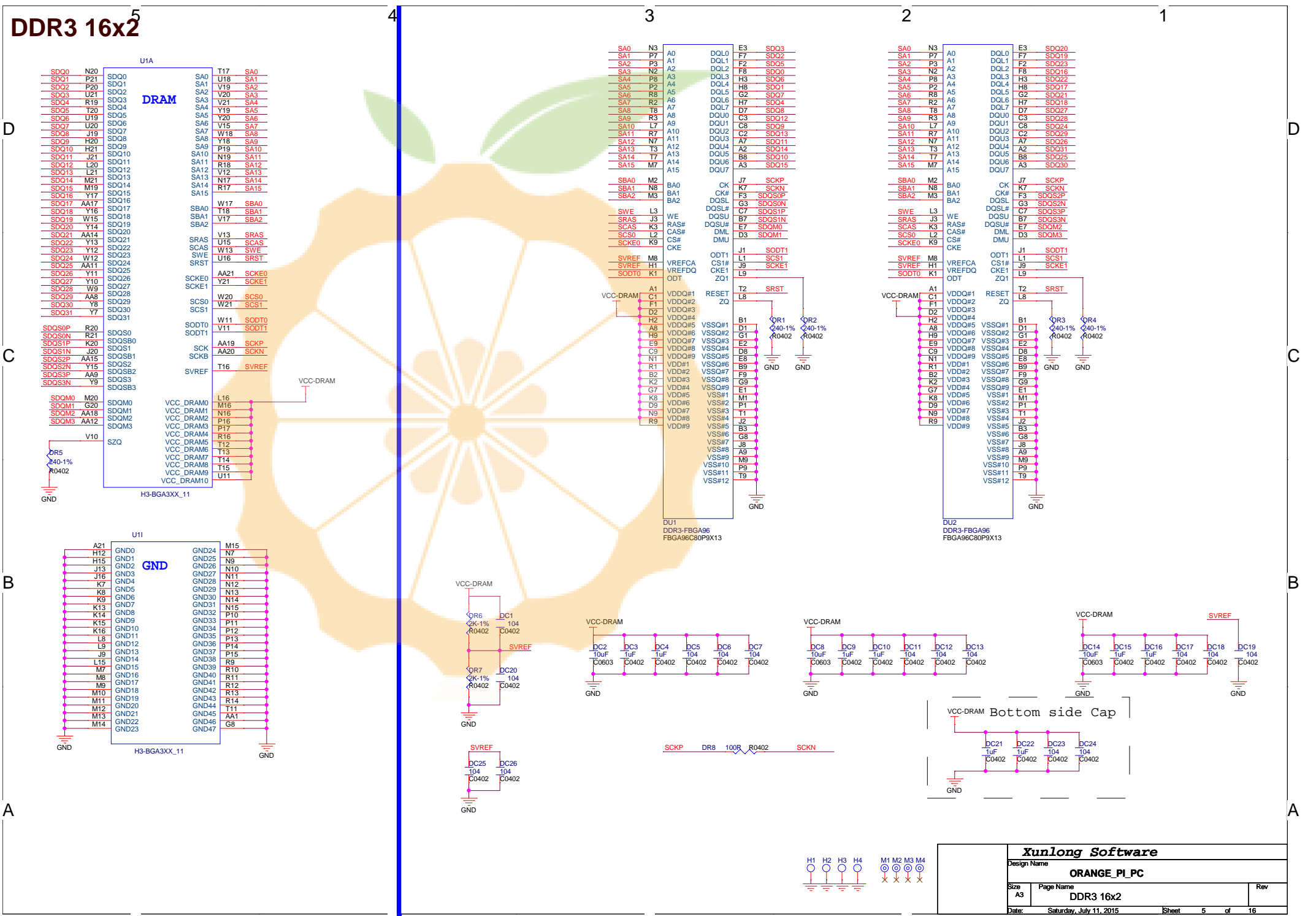
PIN	Define	CFG	Function
PE0	NC	7	
PE1	NC	7	
PE2	NC	7	
PE3	NC	7	
PE4	NC	7	
PE5	NC	7	
PE6	NC	7	
PE7	NC	7	
PE8	NC	7	
PE9	NC	7	
PE10	NC	7	
PE11	NC	7	
PE12	NC	7	
PE13	NC	7	
PE14	NC	7	
PE15	NC	7	

PIN	Define	CFG	Function
PF0	D1	2	CARD0
PF1	D0	2	
PF2	CLK	2	
PF3	CMD	2	
PF4	D3	2	
PF5	D2	2	
PF6	DET	0	

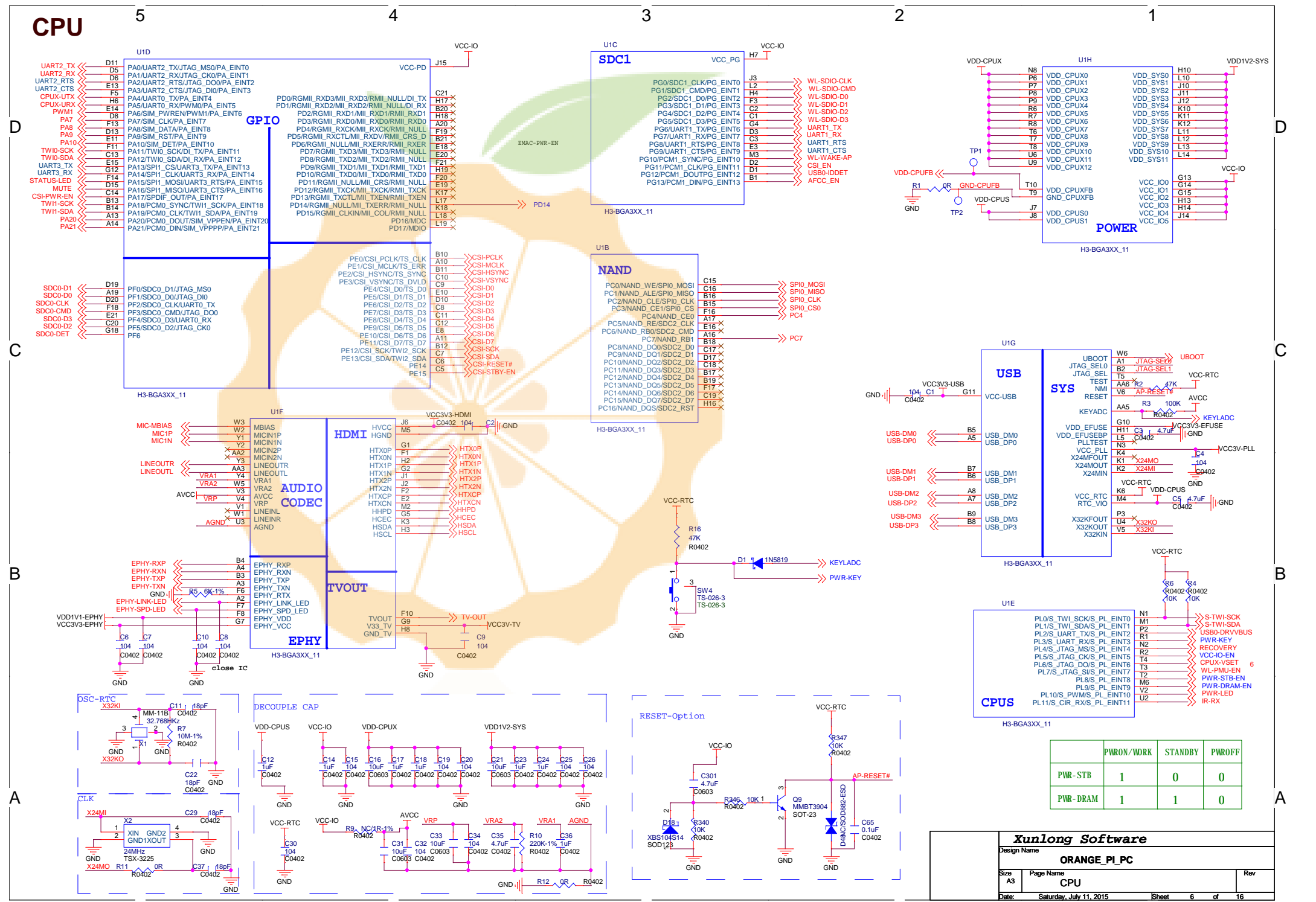
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PG1	NC	7	
PG2	NC	7	
PG3	NC	7	
PG4	NC	7	
PG5	NC	7	
PG6	NC	7	
PG7	NC	7	
PG8	NC	7	
PG9	NC	7	
PG10	NC	7	
PG11	NC	7	
PG12	NC	7	
PG13	NC	7	

PIN	Define	CFG	Function
PL0	TWI	2	TWI
PL1	TWI	2	TWI
PL2	USB0-DRVVBUS	1	USB
PL3	USB1-DRVVBUS	1	
PL4	RECOVERY	0	KEY
PL5	VCC-IO-EN	1	IO-EN
PL6	NC	7	
PL7	WIFI-EN	7	WIFI-EN
PL8	PWR-STB	1	
PL9	PWR-DRAM	1	
PL10	PWR-LED	1	
PL11	IR-RX	2	

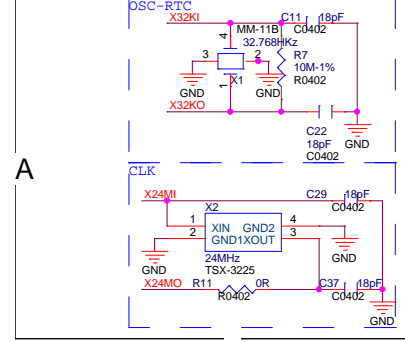
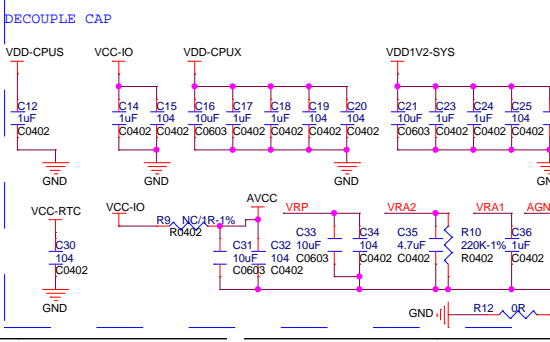
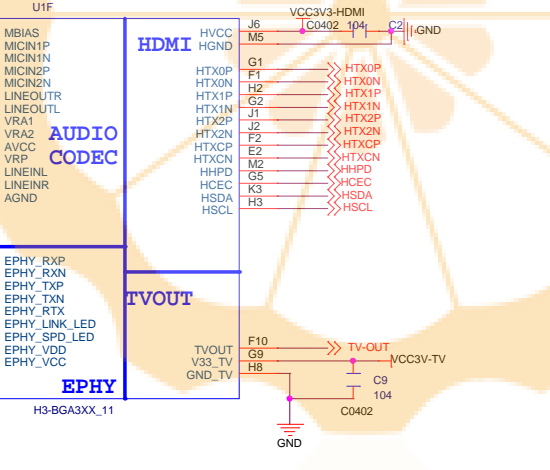
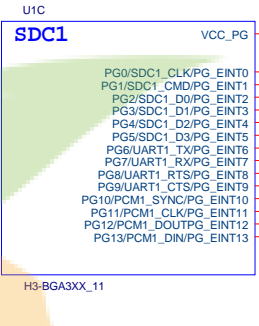
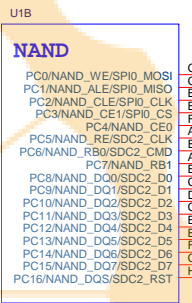
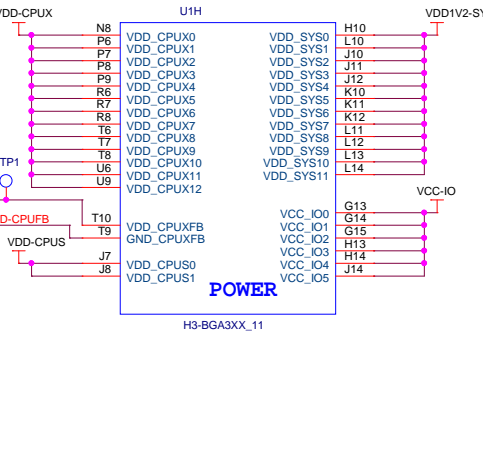
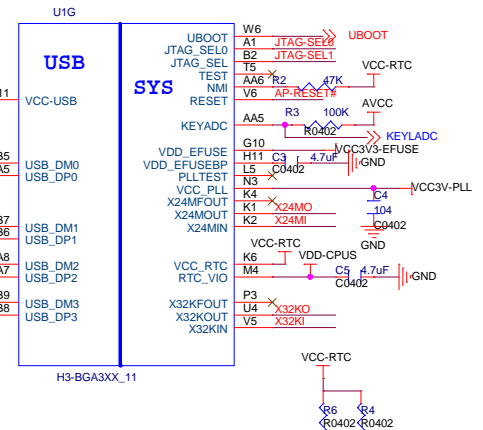
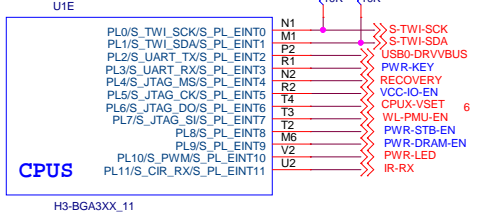
DDR3 16x2



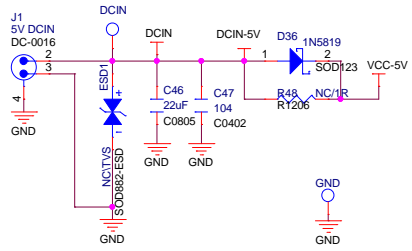
CPU



	PWRON/WORK	STANDBY	PWROFF
PWR-STB	1	0	0
PWR-DRAM	1	1	0



DCIN

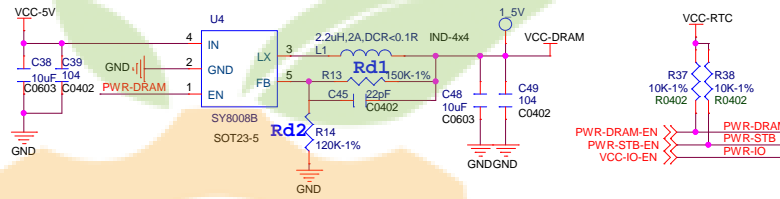


POWER

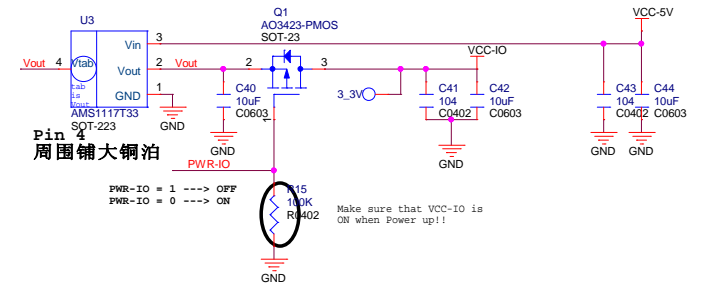
$$V_{out} = 0.6 * (1 + R_{d1} / R_{d2})$$

$$V_{DRAM} = 1.5V / 1A, R_2 = 100K - 1\%$$

$$V_{DRAM} = 1.35V / 1A, R_2 = 120K - 1\%$$

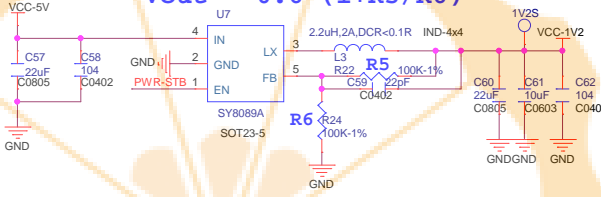


VCCIO 3.3V/1A

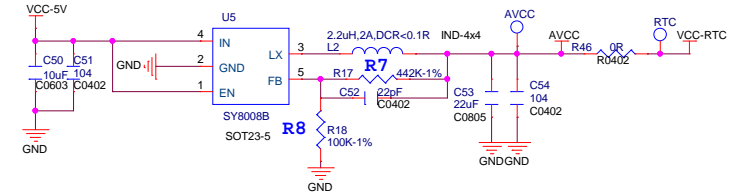


SYSTEM 1.2V/2A

$$V_{out} = 0.6 * (1 + R_5 / R_6)$$

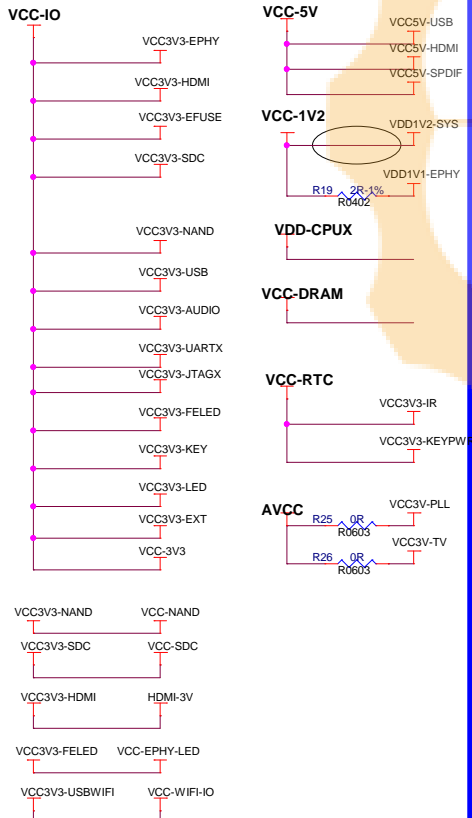
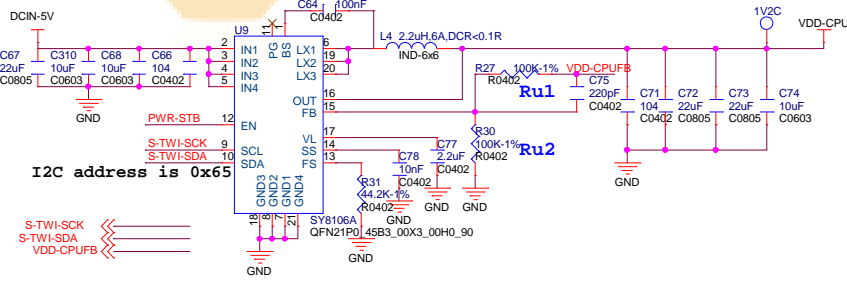


AVCC 3.3V/1A



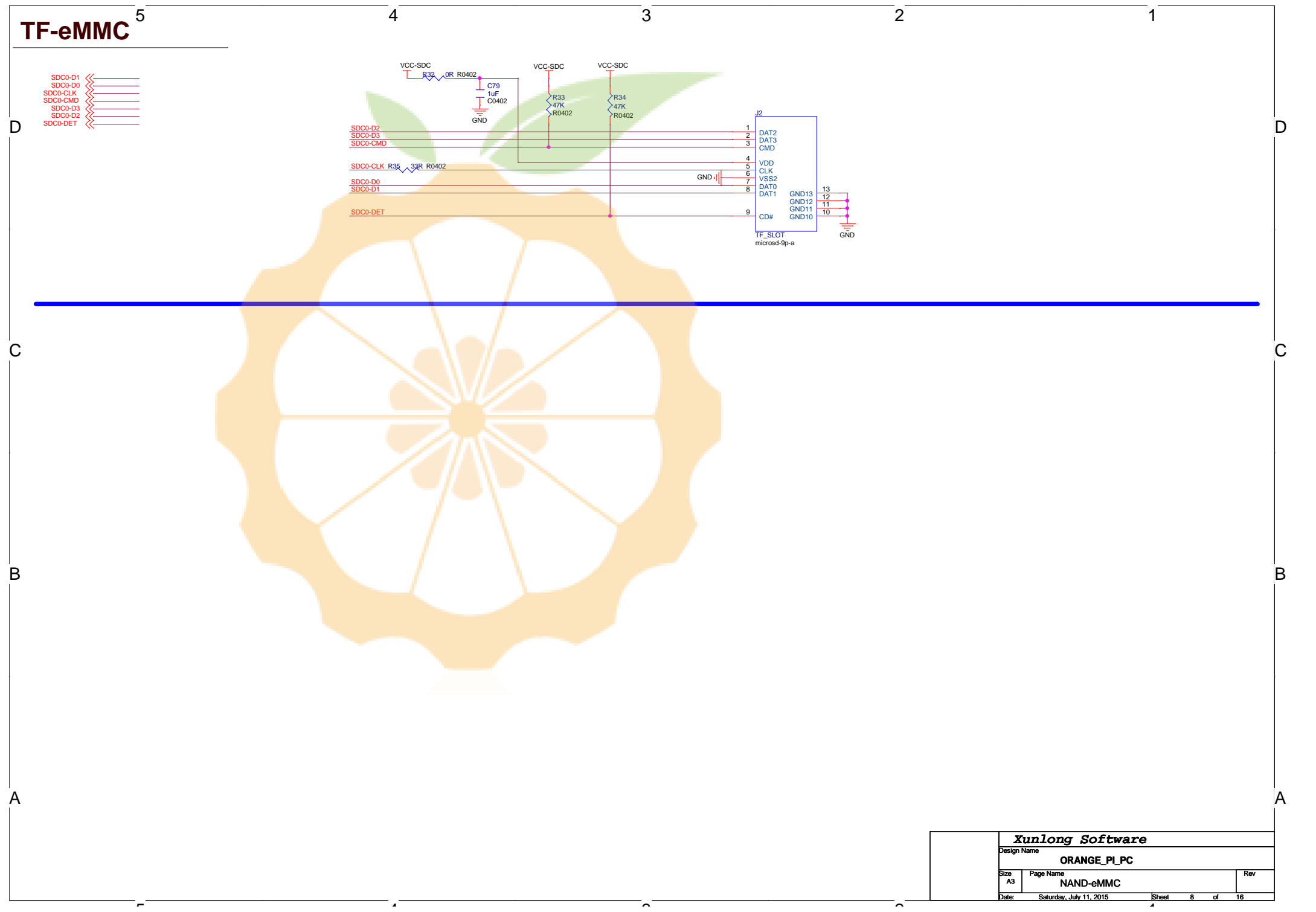
CPUX 1.2V/6A

$$V_{out} = 0.6 * (1 + R_{u1} / R_{u2})$$



Xunlong Software		
Design Name		
ORANGE_PI_PC		
Size	Page Name	Rev
A3	POWER	
Date:	Saturday, July 11, 2015	Sheet 7 of 16

TF-eMMC



Xunlong Software		
Design Name		
ORANGE_PI_PC		
Size	Page Name	Rev
A3	NAND-eMMC	
Date:	Saturday, July 11, 2015	Sheet 8 of 16

USB

5

4

3

2

1

D

D

C

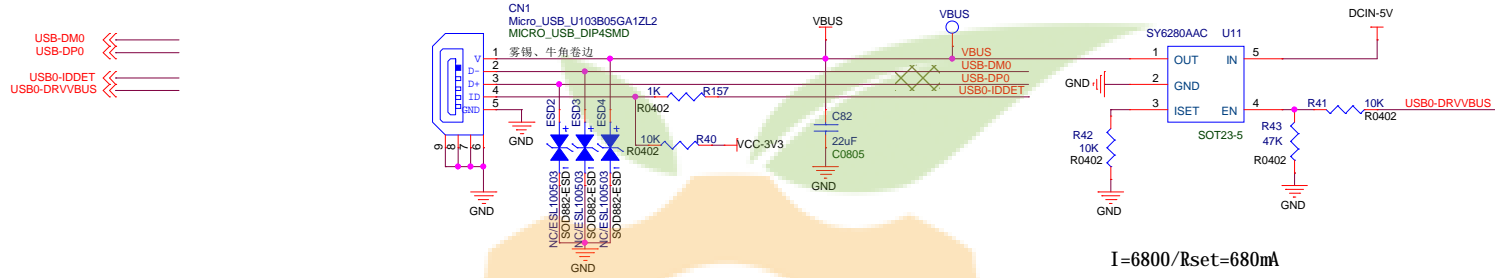
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B

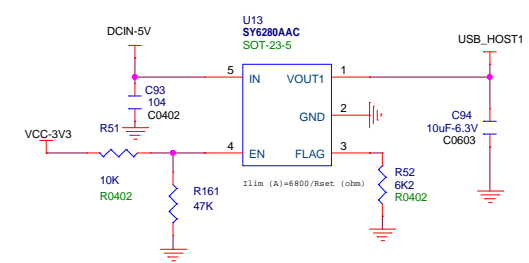
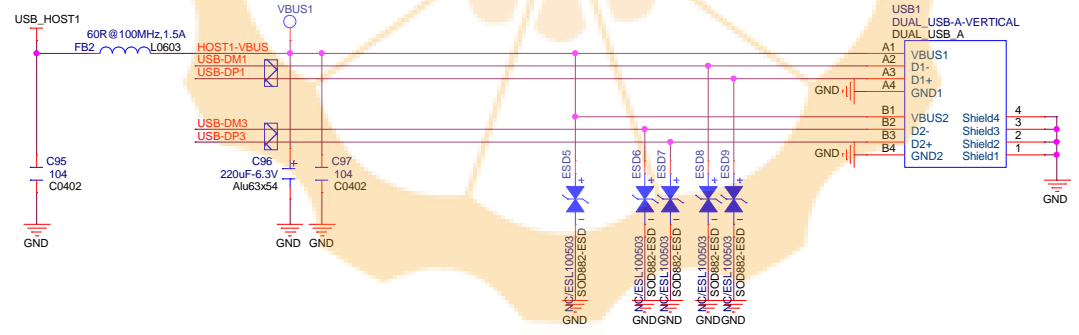
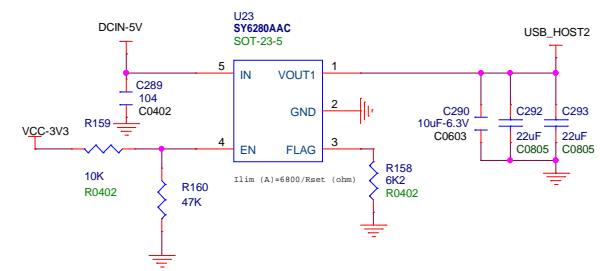
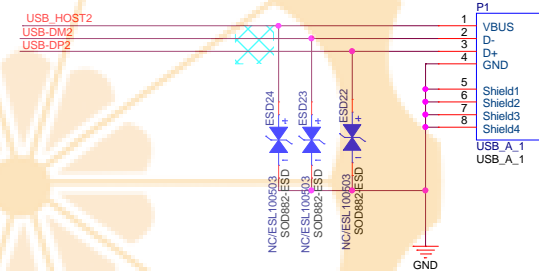
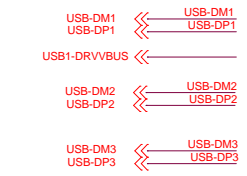
B

A

A

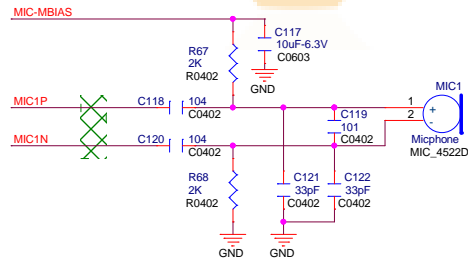
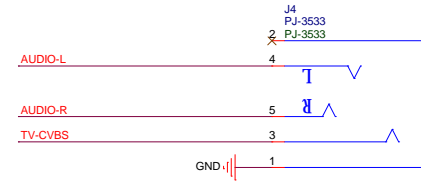
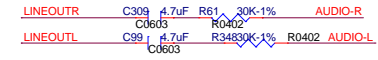
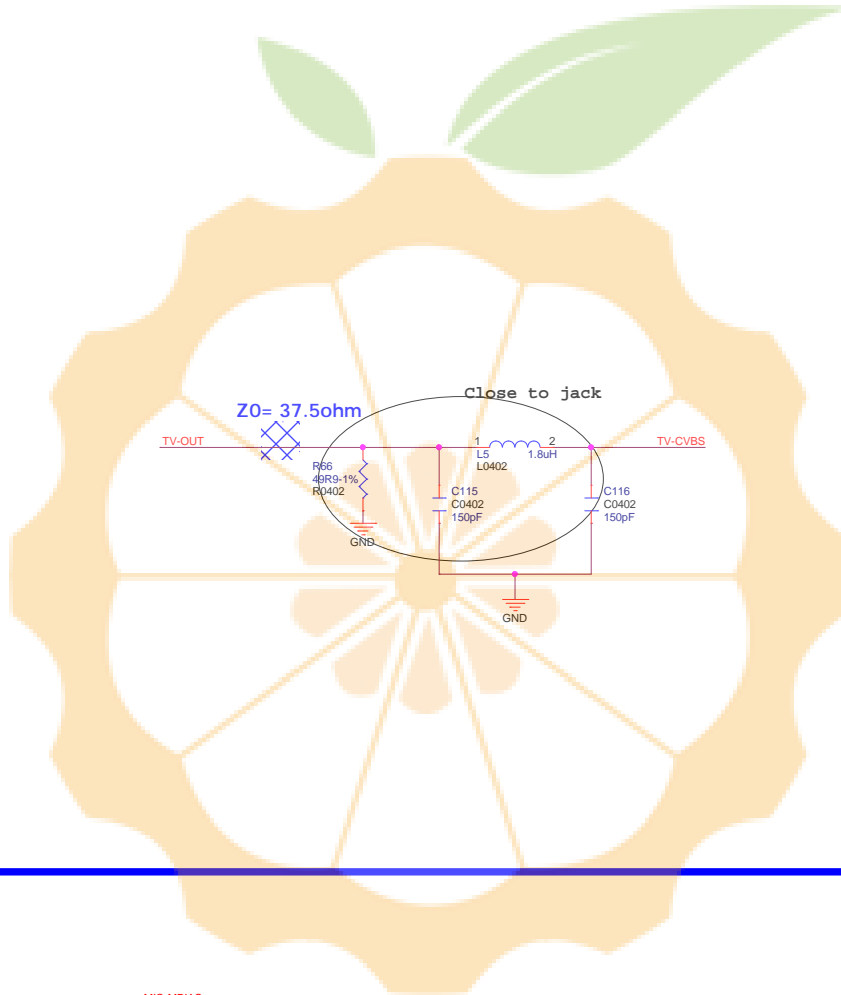
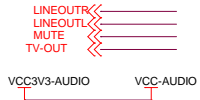


note: Make sure the routing between the ESD and the USB connectors should be on the same PCB side



Xunlong Software		
Design Name ORANGE_PI_PC		
Size A3	Page Name TF-USB-USBWIFI	Rev
Date: Saturday, July 11, 2015	Sheet 9	of 16

AV-MIC



Xunlong Software			
Design Name		ORANGE_PI_PC	
Size	Page Name	Rev	
A3	AV-SPDIF		
Date:	Saturday, July 11, 2015	Sheet	10 of 16

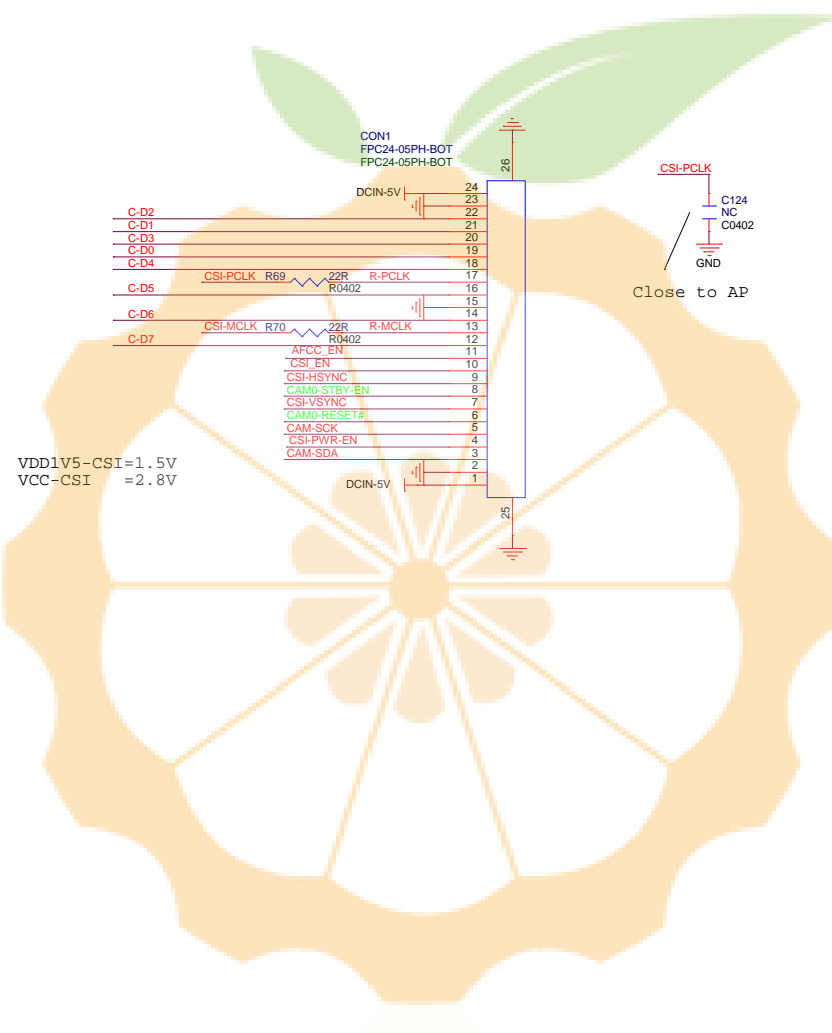
Camera

CSI-RESET# << CAM0-RESET#
 CSI-STBY-EN << CAM0-STBY-EN
 CSI-PWR-EN << CSI-PWR-EN

CSI-SCK << CAM-SCK
 CSI-SDA << CAM-SDA
 CSI-PCLK << CSI-PCLK
 CSI-MCLK << CSI-MCLK
 CSI-HSYNC << CSI-HSYNC
 CSI-VSYNC << CSI-VSYNC

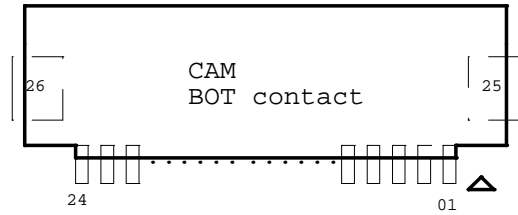
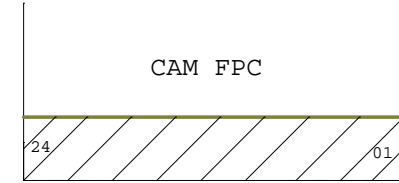
CSI-D0 << C-D0
 CSI-D1 << C-D1
 CSI-D2 << C-D2
 CSI-D3 << C-D3
 CSI-D4 << C-D4
 CSI-D5 << C-D5
 CSI-D6 << C-D6
 CSI-D7 << C-D7

AFCC_EN << AFCC_EN
 CSI_EN << CSI_EN



VDD1V5-CSI=1.5V
 VCC-CSI=2.8V

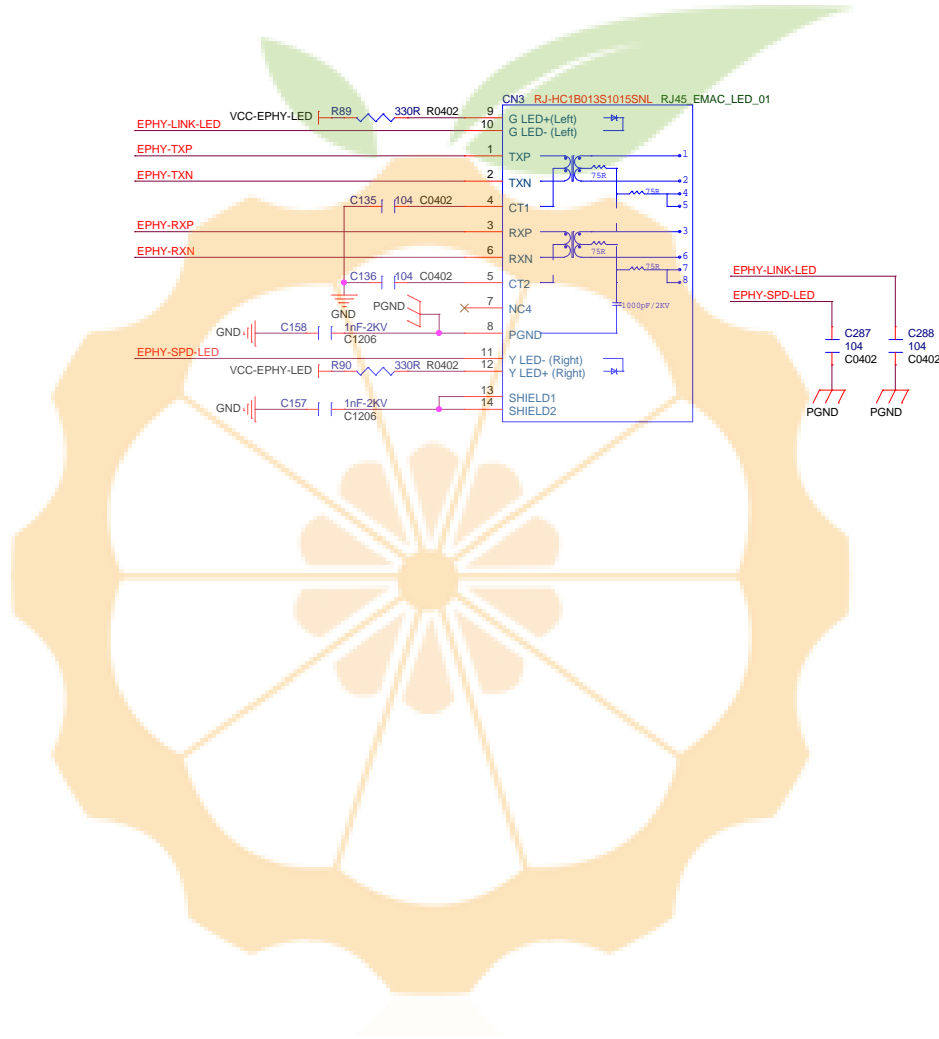
Close to AP



Xunlong Software			
Design Name		ORANGE_PI_PC	
Size	Page Name	Rev	
A3	HDMI-MISC		
Date:	Saturday, July 11, 2015	Sheet	11 of 16

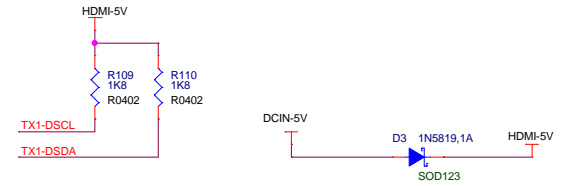
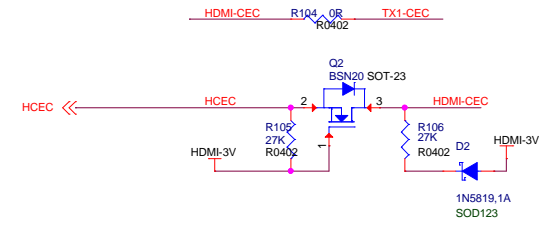
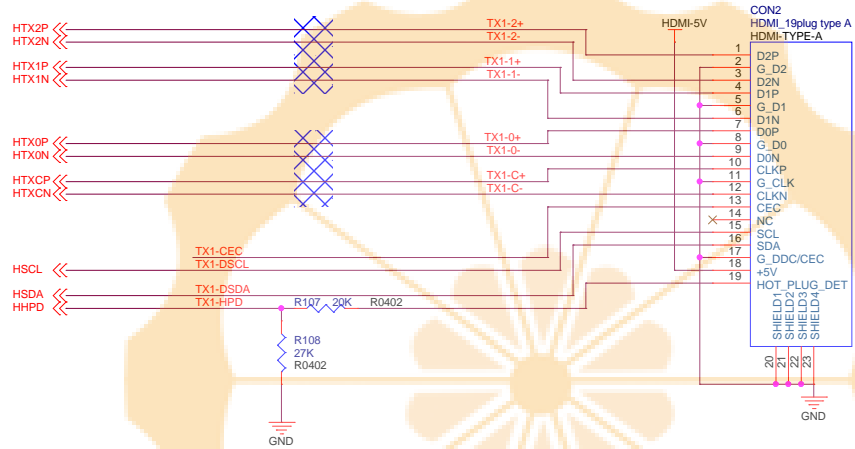
EMAC

- EPHY-RXP
- EPHY-RXN
- EPHY-TXP
- EPHY-TXN
- EPHY-LINK-LED
- EPHY-SPD-LED
- VCC-EPHY-LED



Xunlong Software		
Design Name		
ORANGE_PI_PC		
Size	Page Name	Rev
A3	FE-DBG	
Date:	Saturday, July 11, 2015	Sheet 12 of 16

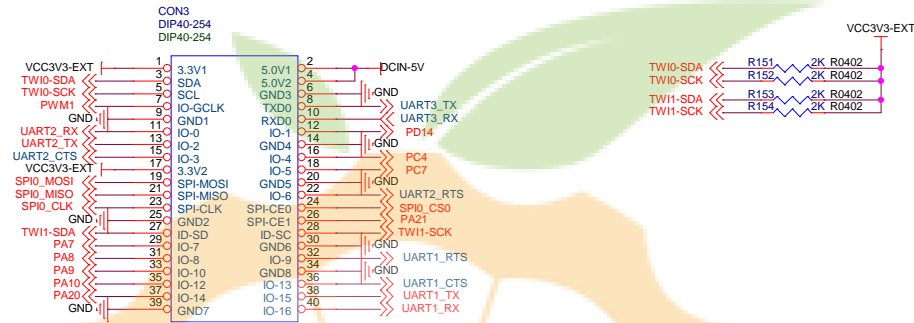
HDMI



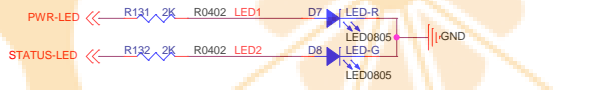
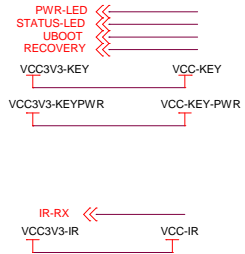
Xunlong Software			
Design Name		ORANGE_PI_PC	
Size	Page Name	Rev	
A3	SiI9612-4K		
Date:	Saturday, July 11, 2015	Sheet	13 of 16

Ext Port

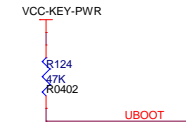
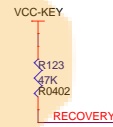
Ext



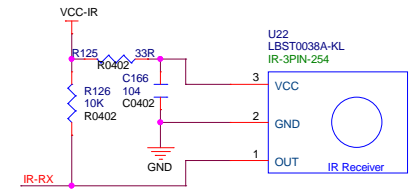
LED



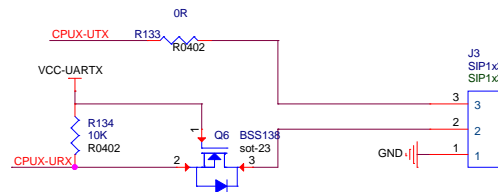
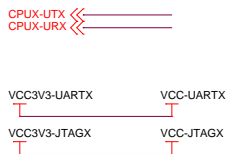
KEY



IR



DEBUG



Xunlong Software		
Design Name		
ORANGE_PI_PC		
Size	Page Name	Rev
A3	FE-DBG	
Date:	Tuesday, September 08, 2015	Sheet 15 of 16